REMARKS

Claims 23-33 and 41-61 are pending in the subject application. Favorable reconsideration in light of the below comments is respectfully requested.

The Obviousness Rejection

Claims 23-33 and 41-61 are pending in the subject application and stand rejected under 35 U.S.C. §103(a) over the combination of Moore (US 2001/0029152 A1) and Ishizaki, *et al.* (US 2001/0041509 A1). This rejection should be withdrawn for at least the following reasons. Pursuant to Section 103, to establish obviousness there must be some suggestion or motivation, either in the cited art or in the knowledge generally available to one of ordinary skill in the art, to modify the cited art or to combine teachings thereof, and the cited art when combined must teach or suggest all claim elements. First, there is no suggestion or motivation to modify Moore or to combine Moore and Ishizaki, *et al.* Second, the purported combination of Moore and Ishizaki, *et al.* does not teach or suggest the claimed invention. Moreover, Ishizaki, *et al.* teaches away from the purported modification.

Independent claim 23 (and similarly independent claims 41 and 52) recites ***embedding one or more isolated electrical resistance members within a semiconductor wafer with integrated circuit features, obtaining resistance values of respective electrical resistance members, and analyzing the resistance values to determine wafer characteristics of (or control) a CMP process***. In the subject Final Office Action (dated October 20, 2004), it is conceded that Moore fails to disclose embedding and utilizing electrical resistance members as recited in the subject claims, but asserted that Ishizaki, *et al.* teaches embedding resistors in workpeices and that it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the references "because Ishizaki, *et al.* teaches that this [embedding resistors in a workpiece] is a useful technique." (*See* Final Office Action, p. 2).

The Examiner references paragraphs [0004] and [0005] of Ishizaki, *et al.* to support the assertion that Ishizaki, *et al.* teaches embedding resistors in a workpiece is a useful technique. However, these paragraphs do not contemplate whether embedding resistors within a workpiece is a useful technique. Rather, paragraphs [0004] and [0005] simply illustrate one type of processing apparatus in which embedded resistors are employed. Moreover, Ishizaki, *et al.* states that this type of processing apparatus is problematic and/or not useful (*See* p.1, ¶ [0010]) and proposes a processing apparatus that teaches away from the embedded resistor technique described in paragraphs [0004] and [0005] (*See* p.1, ¶ [0013]). The proposed processing apparatus employs position sensors (instead of embedded resistors) and position information obtained therefrom to control processing workpeices and to mitigate utilizing embedded resistors and the problems associated therewith. (*See* p.1, ¶¶ [0014]-[0018]).

Since the Examiner solely relies on paragraphs [0004] and [0005], it appears that she has overlooked paragraphs [0010] and [0013]-[0018] of Ishizaki, *et al.* However, paragraphs [0010] and [0013]-[0018] must be considered even though they clearly teach away from using embedded resistors in workpieces. (*See Phillips Petroleum Co. v. U.S. Steel Corp.*, 673 F.Supp. 1278, 1315, (D. Del. 1987) aff'd 865 F.2d 1247 (Fed. Cir. 1989) ("the prior art references relied upon must be considered in their entirety ... Disclosures in the references that diverge from and teach away from the invention cannot be disregarded."); *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d, 1540, 1550 (Fed. Cir. 1983) *citing In re Kuderna*, 426 F.2d 385 (CCPA 1970) ("In its consideration of the prior art, however, the district court erred ... in considering the references in less than their entireties, i.e., in disregarding disclosures in the references that diverge from and teach away from the invention at hand."); MPEP §2141.02). Furthermore, it is improper to pick and choose portions of cited art, excluding portions that teach away, and rely on such portions taken out of context. (*See for example Bausch & Lomb, Inc. v. Barnes-*

Hind/Hydrocurve, Inc., 796 F.2d, 443 (Fed. Cir. 1986)). Thus, it is improper to reject the subject claims based solely on paragraphs [0004] and [0005] taken out of context and to ignore paragraphs [0010] and [0013]-[0018], which teach away from the apparatus described in paragraphs [0004] and [0005] and the purported modification.

Since Moore does not contemplate embedding electrical resistance members in semiconductor wafers with integrated circuit features as recited in the subject claims and Ishizaki, *et al.* teaches away from utilizing embedded resistors to control processing of ceramic workpeices, neither Moore nor Ishizaki, *et al.* provides a teaching, suggestion, motivation or desirability for the purported combination. The mere fact that cited art can be modified does not render the modification obvious unless the cited art suggests the desirability of the modification. (*See In re Mills,* 916 F.2d 680 (Fed. Cir. 1990)). Furthermore, the Federal Circuit consistently holds that cited art that teaches away cannot be used to establish a *prima facie* case of obviousness. (*See McGinley v. Franklin Sports, Inc.,* 262, F.3d 1339, 1354 (Fed. Cir. 2001) (noting "that references that teach away cannot serve to create a prima facie case of obviousness."). *See also In re Haruna*, 249 F.3d 1327, 1335 (Fed. Cir. 2001)). Moreover, even if combined, the result would not render the subject claims obvious since Ishizaki, *et al.* does not make up for the conceded deficiencies of Moore; that is, Ishizaki, *et al.* teaches controlling processing of workpieces through position sensors and information therefrom, Ishizaki, *et al.* does not employ embedded electrical resistence members as recited in the claims.

From the foregoing, it is readily apparent that Moore and/or Ishizaki, et al. do not teach or suggest each and every element of independent claims 23, 41 and 52 (and claims 24-33, 42-51, and 52-61, which respectively depend therefrom).

Independent claim 41 further recites isolating the electrical resistance members ***within disparate layers*** of a semiconductor wafer with integrated circuit features and ***coupling*** such members to form an individual electrical resistance entity across the disparate layers. The Examiner asserts that it would be obvious to one of ordinary skill in

the art at the time of the invention "to isolate the plurality of electrical resistance members within different layers and to couple them to form an individual electrical resistance entity across the different layers in the modified method of Moore in order to increase the sensitivity of the control by using more members." (*See* Final Office Action, p.3). As noted *supra,* Moore is silent regarding embedding electrical resistance members in semiconductor wafers with integrated circuit features and Ishizaki, *et al.* teaches away from both embedding electrical resistors in a workpeice and utilizing signals therefrom to control workpiece processing. Thus, the combination of Moore and Ishizaki, *et al.* cannot teach or suggest isolating such members within disparate layers of a semiconductor wafer with integrated circuit features or coupling the members to form an individual electrical resistance entity as recited in claim 41.

Since the cited art does not teach or suggest embedding electrical resistance members within disparate layers and coupling such members to form an individual electrical resistance entity across the disparate layers, it appears the Examiner is modifying the references *via* employment of applicants' specification on a 20/20 hindsight (blueprint) based reading to provide the missing teaching. (*Interconnect Planning Corporation v. Thomas E. Feil, Robert O. Carpenter, V Band Systems, Inc., and Turret Equipment Corp.*, 774 F.2d 1132, 1138 (Fed. Cir. 1985.) (stating the invention must be viewed not with the blueprint drawn by the inventor, but in the state of the art that existed at the time). *See also Stewart-Warner Corp. v. City of Pontiac, Michigan,* 767 F.2d 1563, 1570 (Fed. Cir.1985)). The rationale proffered to modify and combine Moore and Ishizaki, *et al.* is to achieve benefits identified in applicant's specification. Applicants' representative respectfully submits that this is an unacceptable and improper basis for a rejection under 35 U.S.C. §103. In essence, this rejection is based on an assertion that it would have been obvious to do something not suggested in the art because so doing would provide advantages stated in applicants' specification. This sort of rationale has been condemned by the Court of Appeals for the Federal Circuit. (*See, for example*,

Panduit Corp. v. Dennison Manufacturing Co., 1 USPQ2d 1593 (Fed. Cir. 1987)).

Independent claim 52 further recites forming at least first and second electrical resistance members in ***different directions within a layer*** of a semiconductor wafer with integrated circuit features and utilizing respective resistences to characterize the CMP process. The Examiner asserts that it would be obvious to one of ordinary skill in the art at the time of the invention "to form at least two electrical resistance members in different directions within a layer and to electrically isolate them to form one another in the modified method of Moore in order to increase the sensitivity of the control by using more members." (*See* Final Office Action, p.3). However, Ishizaki, *et al.* teaches away from utilizing embedded resistors and signals obtained therefrom to control workpiece processing as discussed *supra* and, thus, does not make up for the aforementioned deficiencies of Moore. Furthermore, there is no teaching, suggestion or motivation in the cited art to modify Moore to render claim 52 absent utilizing applicants' specification as a 20/20 hind-sight based roadmap to provide the necessary motivation. For at least this reason, Ishizaki, *et al.* cannot teach or suggest forming electrical resistance members in different directions within a layer of a semiconductor wafer with integrated circuit features.

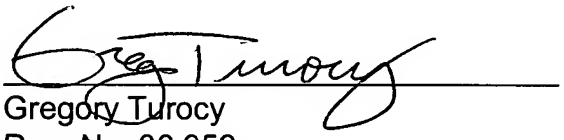
Claims 27, 45 and 59 further recite obtaining at least one of a number of polished semiconductor wafers with integrated circuit features and stiffness associated with the CMP process, and claims 30, 48 and 59 further recite gathering motion information comprising at least one of a motion type, an initial speed, an average speed, a minimum speed and a maximum speed. Neither Moore nor Ishizaki, *et al.* teaches or suggests such elements.

In view of the above, it is respectfully requested that the rejection of claims 23-33 and 41-61 be withdrawn.

Should the Examiner believe that a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact Applicants' undersigned attorney at the telephone number listed below.

In the event any fees are due in connection with the filing of this document, the Commissioner is authorized to charge those fees to our Deposit Account No. 50-1063.

Respectfully submitted,
AMIN & TUROCY, LLP



Gregory Turocy
Reg. No. 36,952

24th Floor, National City Center
1900 East 9th Street
Cleveland, Ohio 44114
(216) 696-8730
Fax (216) 696-8731